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LID#: P12070**CLAIMS:**

- 1           1.       A method of vertically stacking wafers, comprising:  
2               selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers;  
3               bonding the adjacent wafers, via respective metallic lines on opposing surfaces of the adjacent wafers, to  
4       establish electrical connections between active devices on vertically stacked wafers; and  
5               forming one or more vias to establish electrical connections between the active devices on the vertically  
6       stacked wafers and an external interconnect.
- 1           2.       The method as claimed in claim 1, wherein each via is formed by:  
2               selectively etching the top wafer to form a via;  
3               depositing an oxide layer to insulate a sidewall of the via;  
4               forming a barrier/seed layer in the via; and  
5               depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection  
6       between active devices on the vertically stacked wafers and the external interconnect.
- 1           3.       The method as claimed in claim 1, wherein the metallic lines are Copper (Cu) lines deposited to  
2       serve as electrical contacts between active devices on the vertically stacked wafers.
- 1           4.       The method as claimed in claim 2, wherein the conduction metal deposited in the via is copper  
2       (Cu) or a Cu alloy.
- 1           5.       The method as claimed in claim 2, wherein the barrier/seed layer contains a barrier layer deposited  
2       in the via, and a copper (Cu) seed layer deposited in the trench overlying the barrier layer.

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1           6.       The method as claimed in claim 5, wherein the barrier layer is comprised of a material selected  
2       from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and the Cu  
3       seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer by chemical vapor deposition  
4       (CVD) process.

1           7.       The method as claimed in claim 1, further comprising dummy vias arranged on opposing surfaces  
2       of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such  
3       as ground planes or heat conduits for the active devices on the vertically stacked wafers.

1           8.       The method as claimed in claim 1, wherein the vias are formed tapered from the top to the bottom  
2       via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

1           9.       The method as claimed in claim 1, wherein each via is formed by a dual damascene process  
2       comprised of:  
3               selectively etching the top wafer to form an upper trench section of a via;  
4               depositing an oxide layer to insulate a sidewall of the upper trench section of the via;  
5               selectively etching the oxide layer in the upper trench section of the via to form a lower trench section of  
6       the via;  
7               depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and  
8               depositing a conduction metal on the barrier/seed layer for providing an electrical connection between  
9       active devices on the vertically stacked wafers and an external interconnect.

1           10.      The method as claimed in claim 9, wherein the barrier/seed layer includes a barrier layer  
2       comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium  
3       (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench  
4       section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier

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5 layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the  
6 via.

1 11. The method as claimed in claim 1, wherein the vias are formed during a Shallow Trench Isolation  
2 (STI) process in the top wafer before the adjacent wafers are bonded, via the respective metallic lines deposited on  
3 opposing surfaces of the adjacent wafers.

1 12. A method of forming vertically stacked wafers, comprising:  
2 depositing a plurality of metallic lines on opposing surfaces of top and bottom wafers;  
3 forming a conductive plug;  
4 bonding the adjacent wafers, via respective metallic lines, to form vertically stacked wafers; and  
5 forming at least one via on the top wafer to establish electrical connections between the active devices on  
6 the vertically stacked wafers and an external interconnect, by selectively etching through the top wafer until stopped  
7 by the conductive plug, depositing an oxide layer to insulate a sidewall of the via, depositing a barrier/seed layer on  
8 the bottom of the via, and filling the via with a conduction metal to serve as electrical connections between active  
9 devices on the vertically stacked wafers and the external interconnect.

1 13. The method as claimed in claim 12, wherein the metallic lines are Copper (Cu) lines deposited to  
2 serve as electrical contacts between active devices on the vertically stacked wafers.

1 14. The method as claimed in claim 12, wherein the conduction metal deposited in the via is copper  
2 (Cu) or a Cu alloy.

1 15. The method as claimed in claim 12, wherein the barrier/seed layer contains a barrier layer  
2 deposited in the via, and a copper (Cu) seed layer deposited in the via overlying the barrier layer.

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1 16. The method as claimed in claim 15, wherein the barrier layer is comprised of a material selected  
2 from one of the group including tantalum, titanium, and tungsten, and the Cu seed layer is comprised of a few layers  
3 of copper (Cu) atoms deposited on the barrier layer by chemical vapor deposition (CVD) process.

1 17. The method as claimed in claim 12, further comprising dummy vias arranged on opposing  
2 surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary  
3 structures such as ground planes or heat conduits for the active devices on the vertically stacked wafers.

1 18. The method as claimed in claim 12, wherein the via is formed tapered from the top to the bottom  
2 via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

1 19. A three-dimensional (3-D) vertically stacked wafer system, comprising:  
2 a first wafer including an active region to support one or more integrated circuit (IC) devices;  
3 a second wafer including an active region to support one or more integrated circuit (IC) devices;  
4 metallic lines deposited on opposing surfaces of the first and second wafers at designated areas to establish  
5 metal bonding between the first and second wafers in a stack and provide electrical connections between active IC  
6 devices on the first and second wafers in the stack; and  
7 one or more vias formed, via the active region of the first wafer, to serve as electrical connections between  
8 the active IC devices on the first and second wafers in the stack and an external interconnect.

1 20. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 19, wherein the  
2 metallic lines include Copper (Cu) lines deposited on opposing surfaces of the first and second wafers to serve as  
3 electrical contacts between active IC devices on the first and second wafers.

1 21. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each  
2 via is formed by:

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3 selectively etching the first wafer to form a via;  
4 depositing an oxide layer to insulate a sidewall of the via;  
5 forming a barrier/seed layer in the via; and  
6 depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection  
7 between active IC devices on the vertically stacked wafers and the external interconnect.

1 22. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 21, wherein the  
2 conduction metal deposited in the via is copper (Cu) or a Cu alloy, and the barrier/seed layer includes a barrier layer  
3 deposited in the via overlying the oxide layer and a copper (Cu) seed layer deposited in the via overlying the barrier  
4 layer.

1 23. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 22, wherein the  
2 barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride  
3 (Ta<sub>2</sub>N<sub>3</sub>), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited  
4 on the barrier layer by chemical vapor deposition (CVD) process.

1 24. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each  
2 via is formed by a dual damascene process comprised of:  
3 selectively etching the top wafer to form an upper trench section of the via;  
4 depositing an oxide layer to insulate a sidewall of the upper trench section of the via;  
5 etching the oxide layer in the upper trench section to form a lower trench section of the via;  
6 depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and  
7 depositing a conduction metal on the barrier/seed layer for providing an electrical connection between  
8 active devices on the vertically stacked wafers and the external interconnect.

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1           25.     The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 24, wherein the  
2     barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum  
3     (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the  
4     oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper  
5     (Cu) deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the  
6     lower trench section of the via.

1           26.     The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein the  
2     vias are formed during a Shallow Trench Isolation (STI) process in the first wafer before the first and second wafers  
3     are bonded, via the respective metallic lines deposited on opposing surfaces of the first and second wafers.

1           27.     A three-dimensional (3-D) vertically stacked wafer system, comprising:  
2         a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited on opposing  
3         surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and  
4         provide electrical connections between active IC devices on the adjacent wafers;  
5         a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited on opposing  
6         surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and  
7         provide electrical connections between active IC devices on the adjacent wafers; and  
8         one or more vias formed on opposing surfaces of the first stack of wafers and the second stack of adjacent  
9         wafers to serve as electrical connections between the active IC devices on the first and second stacks of wafers and  
10        an external interconnect.

1           28.     The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the  
2     metallic lines include Copper (Cu) lines deposited on opposing surfaces of the adjacent wafers in the first and  
3     second stacks of wafers to serve as electrical contacts between active IC devices on the first and second stacks of  
4     wafers.

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1           29.     The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, further  
2     comprising dummy vias arranged on opposing surfaces of the first and second stacks of adjacent wafers to increase  
3     the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits  
4     for the active IC devices on vertically stacked wafers.

1           30.     The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the  
2     vias are formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding  
3     in the first and second stacks of adjacent wafers.

1           31.     The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein each  
2     via is formed by a dual damascene process comprised of:  
3                 selectively etching the top wafer to form an upper trench section of a via;  
4                 depositing an oxide layer to insulate a sidewall of the upper trench section of the via;  
5                 etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;  
6                 depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and  
7                 depositing a conduction metal on the barrier/seed layer for providing an electrical connection between  
8     active IC devices on the vertically stacked wafers and the external interconnect.

1           32.     The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 31, wherein the  
2     barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum  
3     (Ta), tantalum (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide  
4     layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu)  
5     deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the  
6     lower trench section of the via.